

FIG. 1

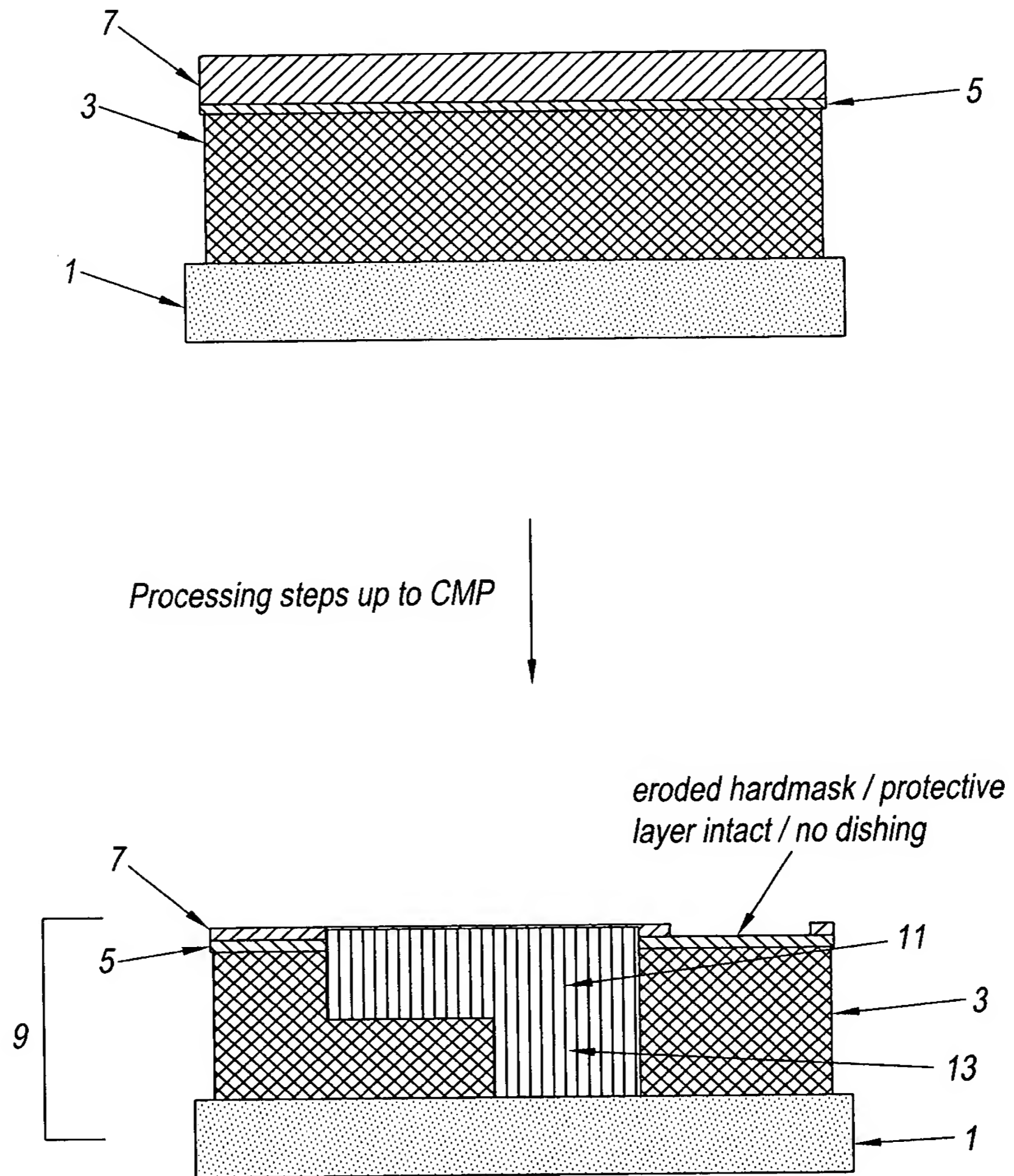


FIG. 2

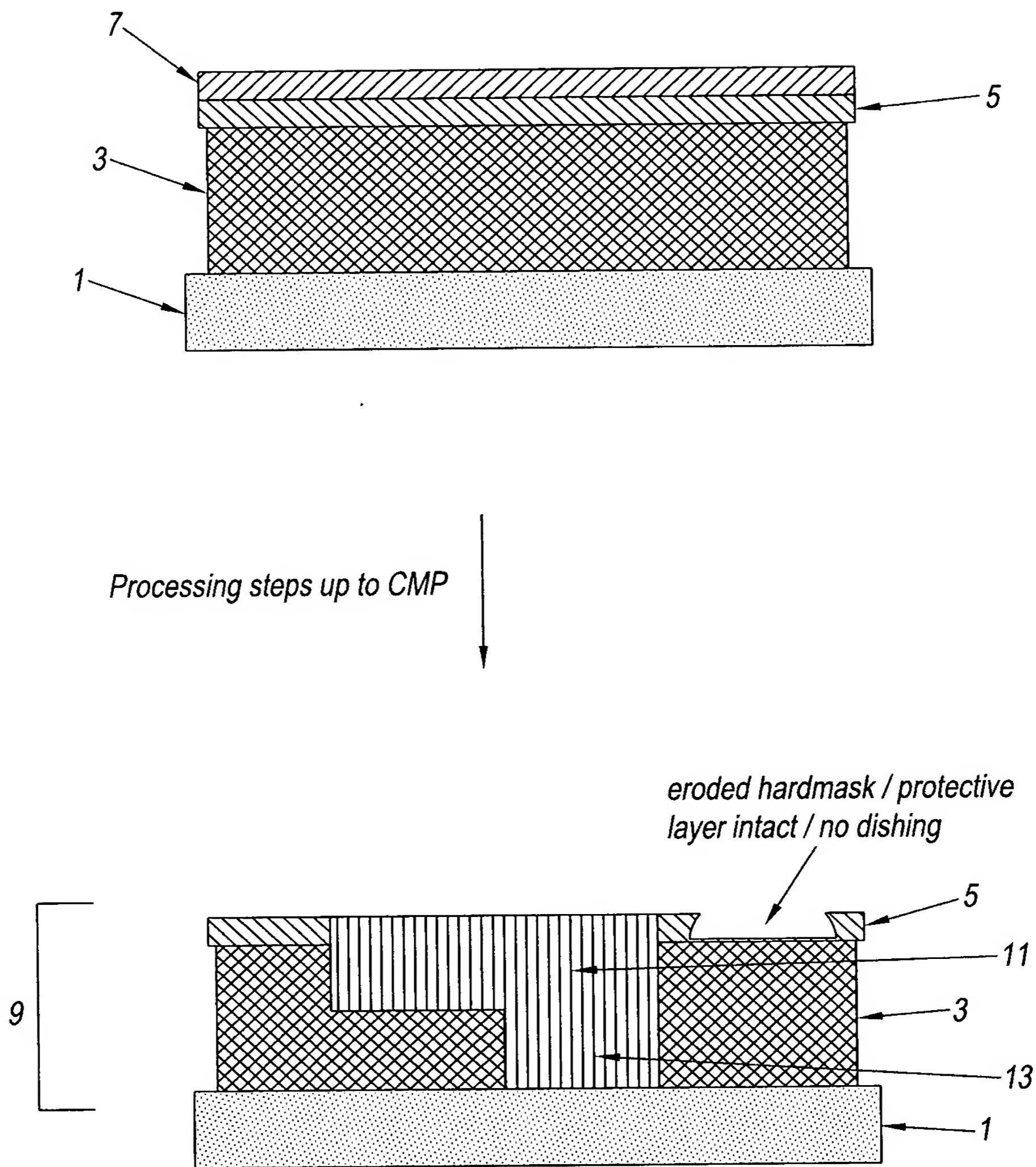


FIG. 3

<i>1) Spin Dielectric layer or layers</i>
<i>2) Hot plate bake dielectric layer to crosslink (310°C, 2 min + 400°C, 2 min)</i>
<i>3) Spin CMP protective layer</i>
<i>4) Hot plate bake CMP protective layer (310°C, 2 min)</i>
<i>5) Furnace Cure multilayer stack (415°C, 1hr)</i>
<i>6) Deposit Hardmask / CMP polish stop layer by conventional CVD methods</i>

FIG. 4